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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Jae Suk LEE**, a citizen of the Republic of Korea, residing at 891-10 Daechi-dong, Gangnam-gu, Seoul, Korea, have invented new and useful **METAL LINE STRUCTURES IN SEMICONDUCTOR DEVICES AND METHODS OF FORMING THE SAME**, of which the following is a specification.

METAL LINE STRUCTURES IN SEMICONDUCTOR DEVICES AND METHODS OF FORMING THE SAME

FIELD OF THE DISCLOSURE

[0001] This disclosure relates generally to semiconductor devices, and, more particularly, to metal line structures in semiconductor devices and methods of forming the same.

BACKGROUND

[0002] As shown in Fig. 1A, a conventional method for forming a metal line sequentially stacks a first Ti/TiN layer 13, a metal layer 15 and a second Ti/TiN layer 17 on a substrate 11. Al is generally used as the metal layer 15.

[0003] Referring to Fig. 1B, a photoresist film is coated on the second Ti/TiN layer 17, and a photoresist pattern 19 is formed by selectively exposing and developing the photoresist film such that a pattern of the photoresist film is left in the areas intended to form metal lines. Such a process is referred to as an embossed patterning method.

[0004] Referring to Fig. 1C, by selectively etching the first Ti/TiN layer 13, the metal layer 15, and the second Ti/TiN layer 17 by using the photoresist pattern 19 as a mask, metal line(s) having a stacked structure including the Ti/TiN layer 13, the metal layer 15 and the Ti/TiN layer 17 is formed. The photoresist pattern 19 is then removed.

[0005] Recently, as semiconductor devices have become more highly integrated, in order to form a metal line having low resistance, a

thickness of the metal line is increased. Further, a pitch of adjacent metal lines is decreased, thereby causing difficulty in forming an interlayer insulator. For resolving such problems, a damascene process using Cu instead of Al as the metal line is employed.

[0006] However, the damascene process using Cu has many problems because a plating process should be performed therein for mass production. Also, if a metal line including Cu is formed on the substrate, a problem occurs wherein Cu ions are diffused on the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figs. 1A to 1C illustrate cross sectional views sequentially showing a conventional method of forming a metal line.

[0008] Figs. 2A to 2I depict cross sectional views sequentially showing an example method of forming a metal line.

[0009] Like reference numerals used in the drawings refer to like parts.

DETAILED DESCRIPTION

[0010] Figs. 2A to 2I are cross sectional views showing an example process of forming a metal line in a semiconductor device. The structure of the metal line formed by the process illustrated in Figs. 2A-2I includes first metal lines 108 (each having a first barrier metal layer 102a and a first conductive layer 104a); a first interlayer insulator 110 filled between the adjacent first metal lines 108; second metal lines 120 (each having a second barrier metal layer 116 and a second conductive layer 118a); and a second

interlayer insulator filled between the adjacent second metal lines, wherein the second metal lines 120 are formed on respective ones of the first metal lines 108.

[0011] Referring to Fig. 2A, the first barrier metal layer 102 and the first conductive layer 104 is sequentially stacked on an insulating substrate 100 having metal line contact holes (not shown). A photoresist film is then coated on the first conductive layer 104. A first photoresist pattern 106 is then formed by an embossed patterning method wherein the photoresist film is removed everywhere except in those areas where it is desired to form the first metal lines. In this process, an Al alloy containing 5% or less Cu is used as the first conductive layer 104 and each of the deposited first metal lines 108 has about 50% of the thickness of a desired metal line structure.

[0012] As shown in Fig. 2B, the first conductive layer 104 and the first barrier metal layer 102 are selectively etched by using the photoresist pattern 106 as a mask, so that the first metal lines 108 are formed with each of the first metal lines 108 including the patterned first barrier metal layer 102a and the patterned first conductive layer 104a. The photoresist pattern 106 is then removed. (see Fig. 2B)

[0013] Referring to Fig. 2C, by using, for example, an HDP (High Density Plasma) process, a first interlayer insulator 110 is formed on the entire substrate 100 and the first metal lines 108 formed on the substrate 100. At this time, because the thickness of each of the first metal lines 108 is small, no void is generated inside of the interlayer insulator 110 and no clipping occurs at the top corners of the first metal lines 108. The first interlayer

insulator 110 formed on the entire substrate may be USG (Undoped Silicate Glass) or FSG (Fluorinated Silicate Glass) deposited by the HDP process.

[0014] As shown in Fig. 2D, by performing a CMP (Chemical Mechanical Polishing) process, an upper part of the first interlayer insulator 110 is removed to expose the top surface of each of the first metal lines 108. In the CMP process, the thickness of the first interlayer insulator 110 becomes less than that of the first metal lines 108, which is a cause of a metal bridge.

[0015] As shown by comparing Figs. 2D and 2E, a metal CMP process is performed in order to eliminate the cause of the metal bridge. By the metal CMP process, a part of each of the first metal lines 108 is removed so as to have the same thickness as the first interlayer insulator 110. As a result, the first metal lines 108 and the first interlayer insulator 110 are evenly flattened.

[0016] Thereafter, as shown in Fig. 2F, a second interlayer insulator 112 is formed on the first metal lines 108 and the first interlayer insulator 110 by performing a PECVD (Plasma Enhanced Chemical Vapor Deposition) process. A photoresist film is coated on the second interlayer insulator 112. The photoresist film is then patterned to expose only areas above the first metal lines 108 to create, a second photoresist pattern 114. At this time, USG or FSG deposited by the PECVD process or PECVD SiOC (Silicon Oxycarbide) is used as the second interlayer insulator 112. The second interlayer insulator 112 has about 50% of the thickness of the desired metal line structure.

[0017] As shown in Fig. 2G, the second interlayer insulator 112 is selectively etched by using the photoresist pattern 114 as a mask until the top surface of each of the first metal lines 108 is entirely exposed. The photoresist pattern 114 is then removed.

[0018] Referring to Fig. 2H, a second barrier metal layer 116 is formed on the etched second interlayer insulator 112. A second conductive layer 118 is then formed on the second barrier metal layer 116, such that the spaces above the first metal lines 108 are filled with the second conductive layer 118. At this time, for example, Cu having a low resistance is used as the second conductive layer 118.

[0019] As shown in Fig. 2I, , the second conductive layer 118 and the second barrier metal layer 116 are removed and planarized by the metal CMP process to expose the top surface of the second interlayer insulator 112. In this way, second metal lines 120 are formed. Each of the second metal lines 120 includes the second barrier metal layer 116 and the planarized second conductive layer 118a. Therefore, a hybrid metal line having a stacked structure of the first barrier metal layer 102a, the first conductive layer 104a, the second barrier metal layer 116 and the second conductive metal layer 118a is obtained.

[0020] Any one of Ti, TiN, Ta, TaN, W, WN and/or a combination thereof may be used as the first and/or the second barrier metal layer 102a, 116.

[0021] Since the hybrid metal line(s) have a stacked structure of an Al alloy and Cu, the metal line(s) have low resistance. Further the Cu

portion of the metal line(s) is formed separated from the substrate 100, thereby preventing Cu ions from being diffused into the substrate.

[0022] From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed methods and apparatus provide a metal line in a semiconductor device and a method for forming the same, wherein the metal line has low resistance and prevents Cu ions from being diffused into the substrate.

[0023] From the foregoing, persons of ordinary skill in the art will further appreciate that methods for forming a metal line structure on a substrate have been disclosed. A disclosed method includes: forming first metal lines, each having a first barrier metal layer and a first conductive layer; forming a first interlayer insulator on the substrate and the first metal lines; planarizing the first interlayer insulator by removing a part of the interlayer insulator to expose a top surface of each of the first metal lines; forming a second interlayer insulator on the first interlayer insulator and the first metal lines; selectively etching the second interlayer insulator to expose the top surface of each of the first metal lines; forming a second barrier metal layer and a second conductive layer sequentially on the etched second interlayer insulator and the first metal lines; and planarizing the second conductive layer and the second barrier metal layer to expose a top surface of the second interlayer insulator, thereby forming second metal lines each having the second barrier metal layer and the second conductive layer.

[0024] Persons of ordinary skill in the art will further appreciate that, metal line structures formed in a semiconductor device have been disclosed.

A disclosed metal line structure includes: first metal lines, each having a first barrier metal layer and a first conductive layer formed on a substrate; a first interlayer insulator filled between the adjacent first metal lines; second metal lines, each having a second barrier metal layer and a second conductive layer, the second metal lines being respectively formed on the first metal lines; and a second interlayer insulator filled up between the adjacent second metal lines.

[0025] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.